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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,737	12/14/2001	Kazuaki Ano	TI-33183	8828

7590 10/24/2002

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	10/017,737	ANO, KAZUAKI	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE f this c mmunication appears on the c ver sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the application filed December 14, 2001.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10, drawn to a semiconductor structure for a multichip module, classified in class 257, subclass 678.

II. Claims 10-17, drawn to the method for arranging a plurality of integrated chips in a multichip module, classified in class 438, subclass 106.

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

A telephone call was placed to Mike Skrehot on October 9, 2002 which resulted in a provisional election being made without traverse to prosecute the semiconductor structure for a multichip module, claims 1-10. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

4. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6 and 8-10 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art in view of Takiar et al. (U.S. Patent No. 5,495,398).

In regards to claim 1, Applicant's Prior Art discloses the following:

a) a first chip (10) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (See Figure 1 and Page 2 Lines 7 and 8); and

b) a second chip (30) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (See Figure 1 and Page 2 Lines 7 and 8).

In regards to claim 1, Applicant's Prior Art fails to disclose the following:

a) a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip.

However, Takiar et al. ("Takiar") discloses the use of attach areas that have the same area as the chip (See Figure 1 and Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of attach areas that have the same area as the chip as disclosed in Takiar because it aids in providing an electrical connection among the various components.

In regards to claim 2, Applicant's Prior Art fails to disclose the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately 10 *u*m.

However, the applicant has not established the critical nature of the dimension of 10 *u*m. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 3, Applicant's Prior Art fails to disclose the following:

a) first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

However, Takiar discloses the use of a thermosetting material (See Column 5 Lines 38-52). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of thermosetting material as disclosed in Takiar because it aids in providing an connection among the chips.

In regards to claim 4, Applicant's Prior Art discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas (See Figure 1).

In regards to claim 5, Applicant's Prior Art discloses the following:

a) first chip and said second chip have a stacked arrangement such that said first chip bonding pads are covered from above by said second chip (See Figure 1 and Page 2 Lines 7 and 8).

In regards to claim 6, Applicant's Prior Art fails to disclose the following:

a) a second attach layer having an area equal to said second chip bottom surface area and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip.

However, Takiar discloses the use of a thermosetting material (See Column 5 Lines 38-52). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of thermosetting material as disclosed in Takiar because it aids in providing an connection among the chips.

In regards to claim 8, Applicant's Prior Art discloses the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness (See Figure 1).

In regards to claim 9, Applicant's Prior Art fails to disclose the following:

a) second attach layer thickness is approximately 1 *u*m.

However, the applicant has not established the critical nature of the dimension of 1 *u*m. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 10, Applicant's Prior Art discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas, and wherein said first and second chips are stacked such that said first chip bonding pads are covered from above by said second chip (See Figure 1).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art in view of Takiar et al. (U.S. Patent No. 5,495,398) and Kuramochi (U.S. Patent No. 5,521,122).

In regards to claim 7, Applicant's Prior Art fails to disclose the following:

a) thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

However, Takiar discloses the use of a thermosetting material (See Column 5 Lines 38-52). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the

use of thermosetting material as disclosed in Takiar because it aids in providing an connection among the chips.

b) second attach layer is silicon dioxide.

However, Kuramochi discloses the use of silicon dioxide (See Column 5 Lines 28-31). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art to include the use of silicon dioxide as disclosed in Kuramochi because it aids in keeping the device from shortening out.

Conclusion

15. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Golwalkar et al. (U.S. Patent No. 5,366,933) discloses a method for construction a dual sided; b) Takiar et al. (U.S. Patent No. 5,502,289) discloses a stacked multi chip module; c) Tuckerman et al. (U.S. Patent No. 5,804,004) discloses a stacked devices for multichip module; d) Ball (U.S. Patent No. 5,898,220) discloses a multichip module device; e) Ball (Re. 36,613) discloses a multichip stacked devices; g) Cho (U.S. Patent No. 6,153,928) discloses a substrate for semiconductor package; h) Akram et al. (U.S. Patent No. 6,222,265) discloses a method of constructing stacked packages; i) LoBianco et al. (U.S. Patent No. 6,340,846) discloses making semiconductor packages with stacked dies; and j) Akram (U.S. Patent No. 6,458,625) discloses a multi chip semiconductor package.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where

this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
October 14, 2002

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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